System Clock Prescaler

The Atmel ATmega328P has a system clock prescaler, and the system clock can be divided by setting the Section 8.12.2

“CLKPR – Clock Prescale Register” on page 33. This feature can be used to decrease the system clock frequency and the

power consumption when the requirement for processing power is low. This can be used with all clock source options, and it

will affect the clock frequency of the CPU and all synchronous peripherals. clkI/O, clkADC, clkCPU, and clkFLASH are divided by

a factor.

When switching between prescaler settings, the system clock prescaler ensures that no glitches occurs in the clock system.

It also ensures that no intermediate frequency is higher than neither the clock frequency corresponding to the previous

setting, nor the clock frequency corresponding to the new setting. The ripple counter that implements the prescaler runs at

the frequency of the undivided clock, which may be faster than the CPU's clock frequency. Hence, it is not possible to

determine the state of the prescaler - even if it were readable, and the exact time it takes to switch from one clock division to

the other cannot be exactly predicted. From the time the CLKPS values are written, it takes between T1 + T2 and

T1 + 2 □ T2 before the new clock frequency is active. In this interval, 2 active clock edges are produced. Here, T1 is the

previous clock period, and T2 is the period corresponding to the new prescaler setting.

To avoid unintentional changes of clock frequency, a special write procedure must be followed to change the CLKPS bits:

- 1. Write the clock prescaler change enable (CLKPCE) bit to one and all other bits in CLKPR to zero.
- 2. Within four cycles, write the desired value to CLKPS while writing a zero to CLKPCE.

Interrupts must be disabled when changing prescaler setting to make sure the write procedure is not interrupted